

### **REMARKS**

The December 13, 2002 Office Action rejects claims 7, 9, 27, and 28; claims 1-6, and 10-26 are withdrawn as being drawn to non-elected species. The present Amendment and Response amends claims 7 and 9. Applicant reserves the right to pursue the subject matter of the withdrawn claims. After entry of this Amendment, claims 7, 9, 27, and 28 remain pending in the application. No new subject matter is being added by this Amendment.

### **Claim Rejections**

Claims 7, 9, 27, and 28 stand rejected under 35 U.S.C 103(a) as being unpatentable over Applicant's admitted prior art in view of United States Patent Number 6, 075, 427, issued to Tai et al. on June 13, 2000 (Tai et al.). Applicant respectfully traverses this rejection.

The present invention provides an improved RF circuit that includes a first metal wiring layer, a dielectric layer overlying the first wiring metal layer, and a second wiring layer overlying a portion of the dielectric layer. The first wiring metal is electrically connected to a via-hole having a metal film on an inside wall of the via-hole. This circuit is illustrated in FIGS. 3A-3C.

The claimed invention set forth in claims 7, 9, 27, and 28 includes a wiring metal layer and an inductor of metal film that are disconnected from each other near the via-hole. This enables one to structure a capacitance by means of the spiral wiring layer and the spiral inductor metal film, and at the same time, enables one to use the spiral inductor metal film as an inductor. As a result, a layered (3D) LC circuit is achieved. This, in turns increases the integration of the semiconductor circuit formed using the present invention.

Tai et al. generally discloses a multi-chip module including a monolithic resonator made using low-cost silicon technology. The module includes a substrate 12, having overlapping, spiral-shaped metal layers 26, 28. The first and second spiral-shaped layers are connected at their inner portions 32, 26 by via 38, which extends between layers 26, 28 (though dielectric layer 44). This structure causes current to travel in the same spiral direction on both of the spiral-shaped layers 26, 28. Column 3, lines 34-41.

As illustrated in FIGS. 3 and 4 of Tai et al., the two coil layers sandwich the substrate by being respectively placed on the two main surfaces of the substrate, and the two layers are connected at their respective centers with the via. The two conducting layers of the coil are simply electrically connected to each other with a substrate between the two coils. Therefore, with this structure, it is impossible to structure a capacitance having a large capacity suitable for a high frequency (e.g., RF) circuit. The patentability of each of the pending claims is addressed in more detail below.

Claim 7 and claims 27, 28 that depend therefrom are patentable over the cited references because no combination of Tai et al. and the admitted prior art teaches or suggests "a wiring metal layer" and "an inductor of metal film...wherein the spiral wiring metal layer and the spiral inductor metal film are disconnected from each other near the via-hole." Rather, Tai et al. discloses first and second wiring levels connected to each other at the via. Accordingly, Applicant requests that the Examiner withdraw the rejection to claims 7, 27, and 28.


Claim 9 is similarly allowable over the cited references because no combination of the references teaches or suggests "a wiring metal layer" and "an inductor of metal film...wherein the spiral wiring metal layer and the spiral inductor metal film are disconnected from each other near the via-hole." Applicant therefore requests that the Examiner withdraw the rejection to claim 9.

**Conclusion**

In view of the foregoing remarks, Applicant submits that the claims are allowable over the cited reference and earnestly requests allowance of all pending claims. The undersigned requests a phone call if for any reason one or more of the pending claims is considered to not be in condition for allowance.

Respectfully submitted,

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